Verification of Active Front End Converter Using Co-Simulation Technique in the LabVIEW

Bojan Banković, Filip Filipović, Milutin Petronijević, Nebojša Mitrović, Vojkan Kostić

Abstract - This paper provides an overview of a co-simulation methodology for the converter Active Front End control algorithm implementation using a National Instrument's (NI) LabVIEW development environment for visual programming language. It allows a rapid prototyping, design, development, debugging and verification of control algorithm for real hardware module implementation, such as a Field-Programmable Gate Array (FPGA). The complete system was verified and optimised before being implemented in the hardware using the NI Multisim simulation plugin for the LabVIEW graphical programming environment. A case study is presented to demonstrate the co-simulation between a Voltage Source Inverter (VSI), LC filter and load side models in the Multisim and standalone control algorithm in the LabVIEW.

Keywords – Active Front End, control algorithm, co-simulation, Field Programmable Gate Array, LabVIEW, Multisim.

I. INTRODUCTION

The approach of design, prototype and deploy embedded control and monitoring systems is significantly changed in the past decade. It became necessary due to increased complexity in design to take extensive analysis and simulations prior to the first prototype build. The advancements in power electronic lead to the emergence of advanced hardware devices with possibilities for the development of new control algorithms [1]. The time needed to select the most optimal solution in such situations can be long and the choice may be ineffective. In order to simplify development, testing, validation, increase productivity and reduce time to final product a various software tools solution are presented such as LabView, Matlab, Caspoc, Proteus, solidThinking Embed and Saber.

The application of power electronic devices such as IGBT, especially in the AC motor control, has resulted the Voltage Source Converter (VSC) technology to become the new gold standard in industry [2]. Apart from motor control, new topologies take place in modern distribution systems as a part of distributed power sources [3]. The passive diode rectifier topology became overcome with the new convertor-inverter topology also called Active Front End due to its ability to recovery energy back in the power grid. The number of distributed power sources like photovoltaic solar farms, wind farms, electric cars, and energy storage is significant and combined with household/building appliances resulting a dramatic increase in the number of prosumers ('producer + consumer'). VSI converters cover a wide range of power ratings with increased efficiency at very affordable prices [4]. Simultaneously with hardware development, new control algorithms are emerging and new topologies are conceived. The twenty-first century - the age of energy-efficient devices and new regulations regarding the quality of electricity and CO_2 emissions [5], conditioned the development of new control algorithms. Their task is wide, from the possibility of the bidirectional energy flow control, adequate synchronization to the power grid and to provide grid voltage or power injection support. In addition to the aforementioned, the control algorithm should provide IGBTs switching control that will reduce the losses, perform the data acquisition/processing and ensure the system's immunity to disruptions.

A graphical system design approach is used for modelling, control, signal processing, and algorithm integration. LabVIEW software provides a superior method for design demanding embedded control systems and gives tools for appropriate tasks monitoring. The entire process of the Active Front End (AFE) modelling has been divided into several separate subprojects. Each of them is modelled separately and tested before the final co-simulation and build-in of the FPGA.

II. LABVIEW BASED MODEL ACTIVE FRONT END CONTROL

A. Active Front End control algorithm in the LabVIEW

Converters represent a bridge between renewable energy sources or prosumers at one side and the power grid on the other. They are irreplaceable devices in smart grids and micro networks generating variable/fixed frequency from DC sources or rectifying AC input voltage to the DC voltage for further conversion (e.g. storage or battery charging). The energy conversion is accomplished with two functional modules called the control stage and the power stage. The power processor of the converter is responsible for the power transfer from the input to the output, or vice versa through power stage. The controller is responsible for operating of the switches according to the specific control algorithm, while voltages and currents are measured at the system input or output. The widespread use of the AFE technology and its application is illustrated in the Fig. 1. Its possibility of bidirectional energy flow constitute the most important feature of this topology. DC-link converters connect motor/generator/load side inverters and/or battery storage or photovoltaic chopper with power grid enabling bidirectional energy flow. Such structure can also operate

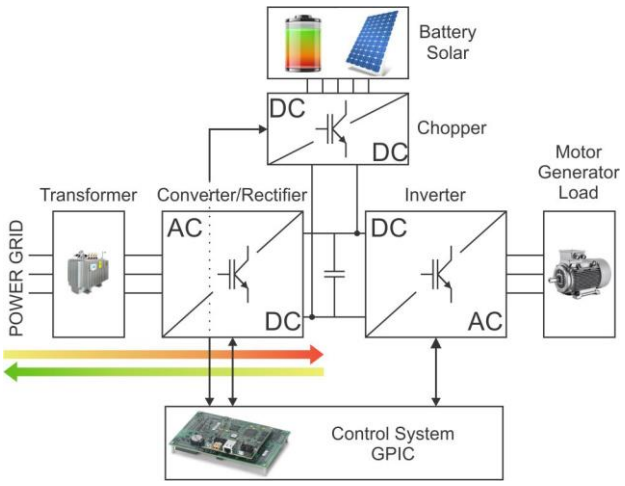

Fig. 1. Active Front End topology in micro grid

as a micro grid with back-to-back converter control strategy for an operation in both stand-alone and grid-connected cases. If we are considering one household/building as a small micro grid, two operating modes are possible. First mode is the stand-alone work regime of the micro grid, where the primary objective of the converter control is to provide desired voltage amplitude and frequency. The second mode is more complex because it requires synchronization of the converter outputs to the main power grid, but also offers more possibilities for various control algorithms.

In the initial stage of control algorithm development, the first mode of operation was taken in consideration. The basic requirements, that the control algorithm should satisfy, are to ensure the stability of the given voltage and frequency in the stand-alone operation. The control algorithm should minimize IGBTs switching losses and provide safe operation (prevents a short-circuit between top and bottom IGBTs in same branch). So extensive testing of the control algorithm should be carried out before the real hardware implementation is performed, in order to ensure functionality of the IGBT switching devices. The principal block-scheme for convertor control algorithm is presented in the Fig. 2.

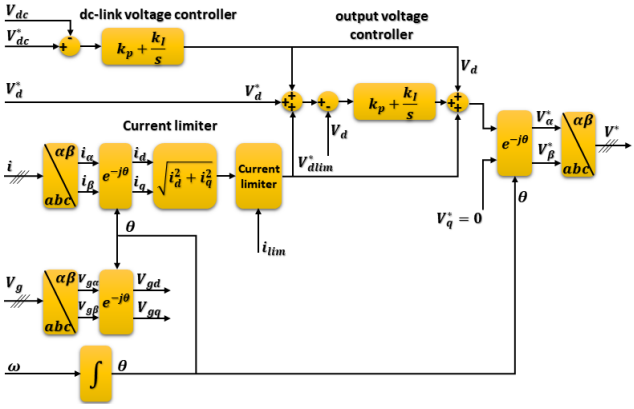

Fig. 2. The control algorithm scheme for the Active Front End converter

LabVIEW provides the convenience of modularity in modelling and programming creating a hierarchical structure of the virtual instruments (VIs) with no limit in the number of layers. Each VI has three components: a block diagram, a front panel and a connector panel. Within LabVIEW, program modularity means creating smaller sections of the control algorithms, known as subVIs. SubVIs are the same as VIs. They contain front panels and block diagrams, but they could be called from a main VI. A subVI is similar to a subroutine in text-based programming languages.

Control algorithm is divided in to several subVIs for easier testing and implementation at different hierarchical levels. An implementation of the control algorithm included three steps. The first one include FPGA development environment for control algorithm execution. The second includes complex mathematical operations and can be performed on the Rael Time platform with DSPs in order to optimize FPGA performance. The third level is the desktop computer for monitoring and control hardware over appropriate application generated in LabVIEW.

SubVIs of the control algorithm are:

- Triangle carrier signal (Triangle.vi) for PWM
- Saw carrier signal (Saw.vi) for PWM
- Dead time implementation for IGBT (DeadTime.vi)
- Filter for electrical signal (SigFilter.vi)
- Calculation angle θ based on ω (ThetaCalc.vi)
- ABC to DQ transformation (ABCtoDQFXP.vi)
- DQ to ABC transformation (DQtoABCFXP.vi)
- PID controller (PIDFXP.vi)

Main VI consists of four structures, which are used in the co-simulation through the FPGA Desktop Execution Node, as it is presented in Fig. 4:

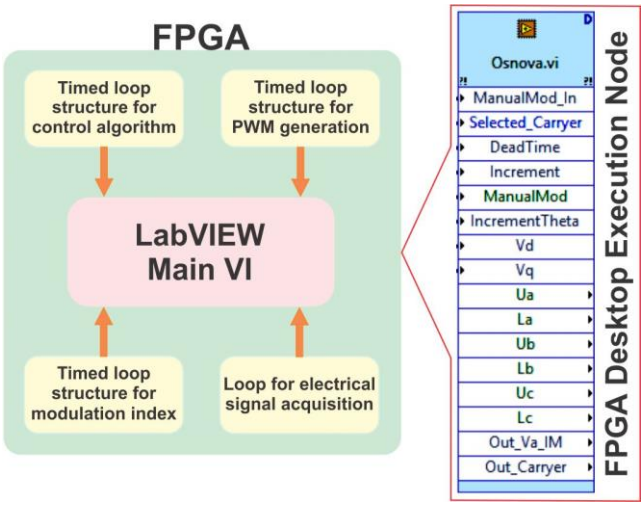

Fig. 4. The control algorithm for the Active Front End converter in the island mode

Before co-simulation is performed, every part of the control algorithm is tested in LabVIEW independently and optimised in respect with execution speed and memory usage. The optimisation is done for an NI Single-Board RIO 9863 Mezzanine with Embedded Device LX45 FPGA

sbRIO-9606. This combination give a possibility of DSP and FPGA usage for control algorithm implementation. Co-simulation is performed using add on LabVIEW Control Design and Simulation Module and NI LabVIEW Co-Simulation Plugin with Multisim in order to evaluate the performance of the control algorithm on the desktop. In order to simulate precise time behaviour of the control algorithm implemented on the FPGA, a discrete time execution rate of the Desktop Execution Node must be configured. This comes at the cost of performance, since a simulation step-size must be chosen to match the 40 MHz FPGA clock period. The simulation tasks was solved using the Runge-Kutta 23 ordinary differential equation (ODE) solver. The control and simulation loops for co-simulation in the form of block diagram is presented on the Fig. 5.

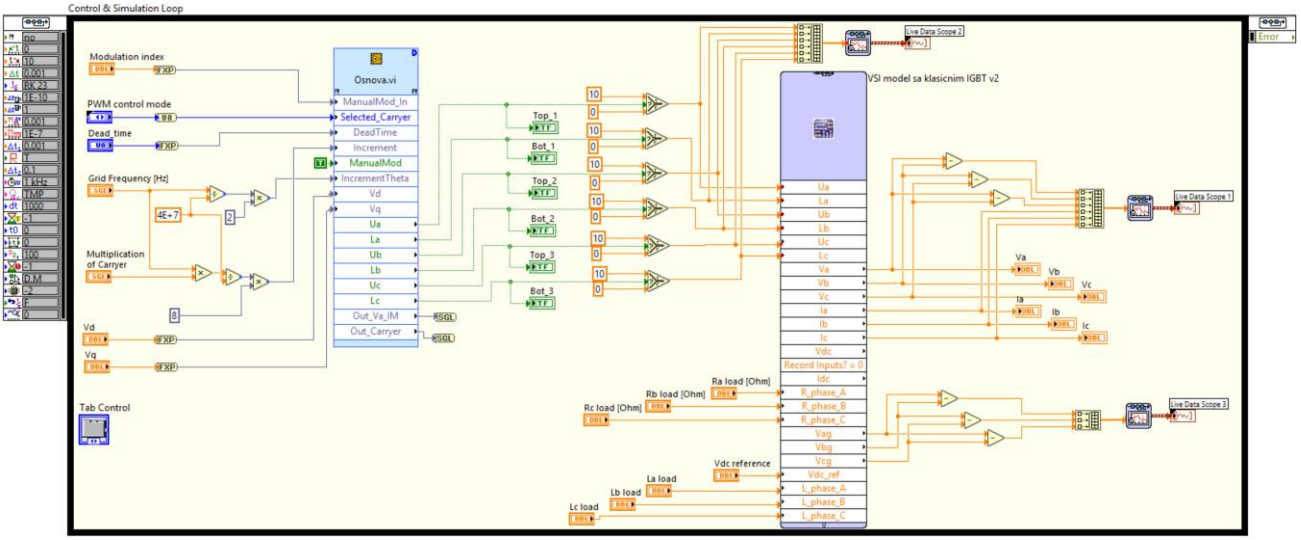

Fig. 5. The control and simulation loops for co-simulation in LabVIEW

B. Voltage Source Inverter, LC filter and load side model in the LabVIEW Multisim

In order to test control algorithm using co-simulation a Voltage Source Invertor (VSI), LC filter and load side model are designed in Multisim. Fig. 6 shows the model used for co-simulation. The load type can be changed from pure active to mixed inductive, in order to observe the current and voltage waveform quality. A reference voltage of the DC link could be set through V_{dcref} and load parameters through $R_{\_phase}$ and $L_{\_phase}$. Measured values for voltages on the output side of the converter and the grid side could be shown with current on the grid side.

The switches S1-S6 where represented with Infineon IGBT model SKM 50GB123D. The gate drivers were not considered in this co-simulation, because their effect on the

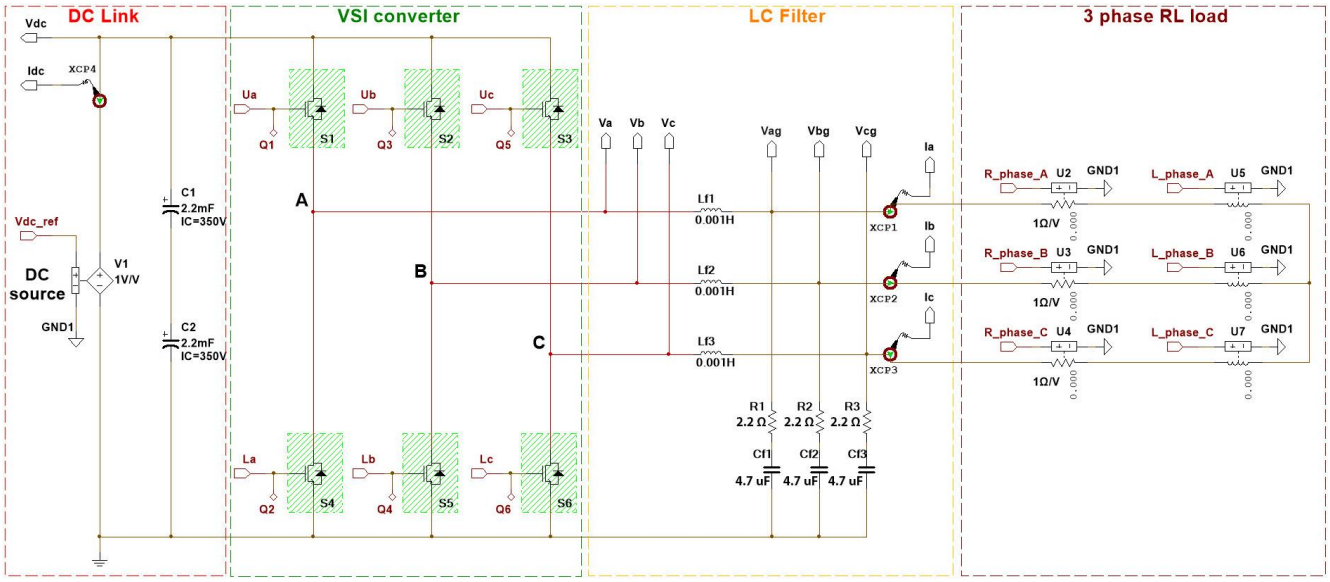

Fig. 6. The power part of the Active Front End converter in the island mode

system dynamic is minimal. The control signals for the IGBTs can be generated through Sine Pulse Width Modulation (SPWM) with saw or triangle carrier. These signals are transmitted to the transistors' gates through the ports U_a, U_b, U_c, L_a, L_b, and L_c. The frequency of the carrier should be select as an integer multiple of the nominal grid frequency f=50 Hz. The LC filter is designed corresponding to the nominal current of the VSI. This current according to the data sheet specification of the IGBTs is 40A for T_{case}=80 °C. In order to calculate inductor L for the filter the current ripple will be defined within ΔI_r=20% of nominal current. According to [6] the inductance L should be selected as:

$$L > 2\frac{U_{dc}}{2\cdot\pi\cdot\sqrt{2}\cdot f_{sw}\cdot 3\cdot\Delta I_r}, \quad (1)$$

where the DC link voltage U_{dc}=650 V and switching frequency f_{sw}=5000 Hz. Adopted value for inductor L is 1.5 mH. This value with nominal grid frequency and nominal load current should produce voltage drop below 10 % of the phase voltage. Voltage drop under rated load is given with:

$$\Delta U = I_n\cdot 2\cdot\pi\cdot f\cdot L \quad (2)$$

The value of the filter capacitors C must provide appropriate resonant frequency f_{res} of the output filter that should satisfy the condition given with Eq. (3) [6]:

$$10\cdot f_{out1h} < f_{res} < \frac{1}{2} f_{sw} \quad (3)$$

For the assumed value of the resonant frequency f_{res}=2000 Hz, the capacitor value C should be calculate with Eq. (4) according to [6]:

$$C = \frac{1}{4\cdot\pi^2\cdot f_{res}^2\cdot L} \quad (4)$$

The nearest standard value of the capacitance C=4.7 μF is selected. For the given parameters L and C, the resonant frequency is given with Eq. (5):

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

and satisfy the condition given with Eq. (3).

Taking into the account the filter quality factor Q=8 for characteristic impedance and damping resistor R_d should be calculated with Eq. (6) and (7) according to [6]:

$$Z_0 = \sqrt{\frac{L}{C}} \quad (6)$$

$$R_d = \frac{Z_0}{Q} \quad (7)$$

The nearest standard value of the resistor is R_d=2.2 Ω.

III. CO-SIMULATION RESULTS

Front end user interface in the LabVIEW co-simulation is presented in the Fig. 7. Through the desktop graphical user interface, it is possible to set the reference values for the grid voltage components and frequency, DC link voltage, dead time for IGBTs and load values in each phase. The measured voltages and currents are shown over the graphic charts while visual presentation of the IGBTs turn on/off state is given. There are also signal charts for the sine PWM signals for each of the six IGBT switches.

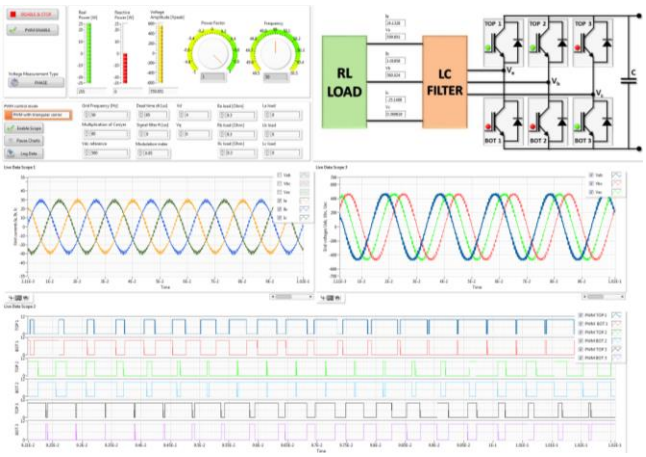

Fig. 7. Front end user interface in the LabVIEW co-simulation

The co-simulation is performed for nominal current of the convertor with the three phase active load of R_{phase}=5.74 Ω and unity power factor. The active power of the consumer is 27.5 kW. An output voltage RMS value from the converter is set to 400 V, grid frequency to 50 Hz, modulation index to 1, dead time of the IGBT to 1.125 μs and the reference DC link voltage to 650 V. In the Fig. 8. instantaneous values of phase currents I_a, I_b, I_c are presented in front of the LC filter. It can be noticed there is no leg shoot through caused with control algorithm. Currents are sinusoidal with frequency of 50 Hz. There is a 20% current ripple of nominal value in the waveform, which makes the current waveform non-ideal sinusoid. In the Fig. 9. instantaneous values of line voltages U_{ab}, U_{bc}, U_{ac} are presented. Voltages at the convertor output in comparison with the voltages in front of the LC filter are smoothed due to the presence of capacitors. Fig. 10. shows generated sine PMW signals with triangular carrier for all six IGBT switches.

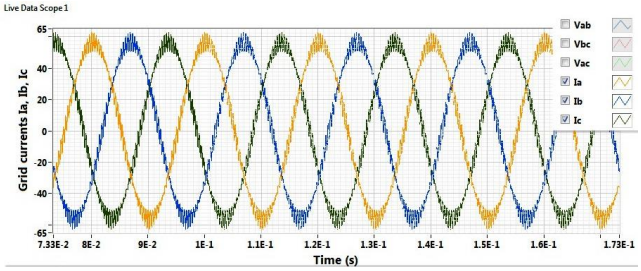

Fig. 8. Waveforms of phase currents I_a, I_b, I_c

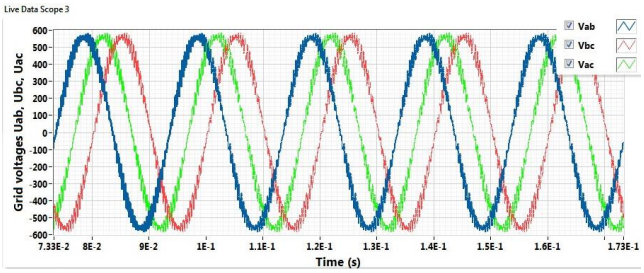

Fig. 9. Waveforms of line voltages U_{ab}, U_{bc}, U_{ac}

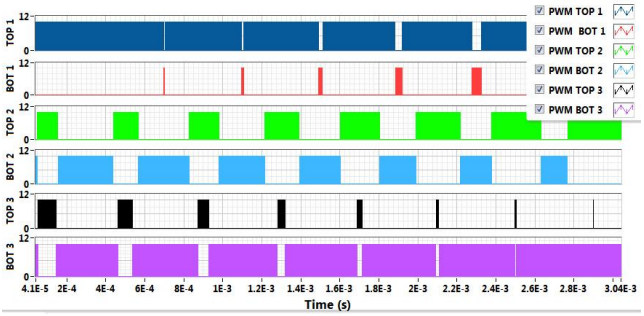

Fig. 10. Generated sine PWM signals

In the second case, a half of the nominal current load is used. It was a three phase active load of R_{phase}=11.4 Ω resistance. In this case, active power of the consumer is around 13.9 kW. The current and voltage waveforms and their instantaneous values are presented in Fig. 11. and 12. It is clear that this control strategy work in conditions of load deviation from nominal ones.

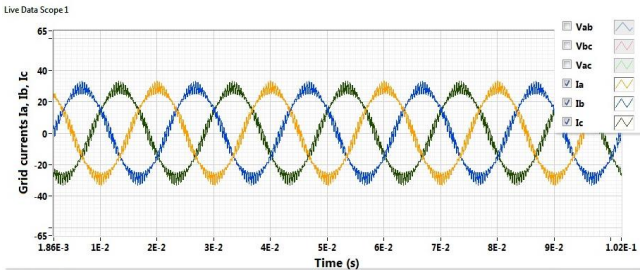

Fig. 11. Waveforms of phase currents I_a, I_b, I_c

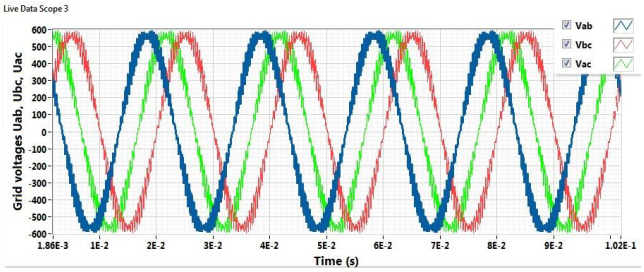

Fig. 12. Waveforms of line voltages U_{ab}, U_{bc}, U_{ca}

The control algorithm and converter model are tested also in the case of the induction load. The load parameters are: phase resistance R_{phase}=4.59 Ω, inductance L_{phase}=11 mH, power factor 0.8 and phase current I_{pRMS}=40 A. The active power of the consumer in this case is 22 kW. The instantaneous values of phase currents I_a, I_b, I_c are shown on the Fig. 13. It could be seen that the current waveforms are almost ideal sinusoid due to value of the inductance L_{phase}. A higher inductance values act as a filter on the current waveforms. Due to the fixed parameters values of the LC filter, which is a real case, the type of the consumer plays a significant role in the current and voltage waveforms. Due to fixed value of capacitance in the LC filter, the consumer load in this case caused a much lower quality voltage waveform. The waveforms of the U_{ab}, U_{bc}, and U_{ac} are presented in Fig. 14.

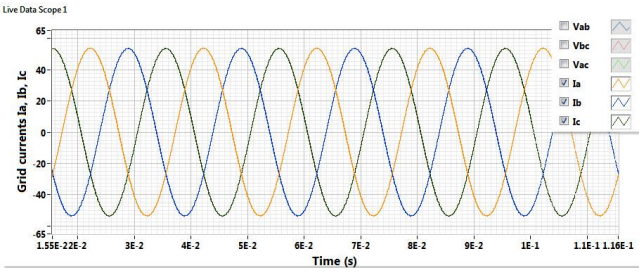

Fig. 13. Waveforms of phase currents I_a, I_b, I_c

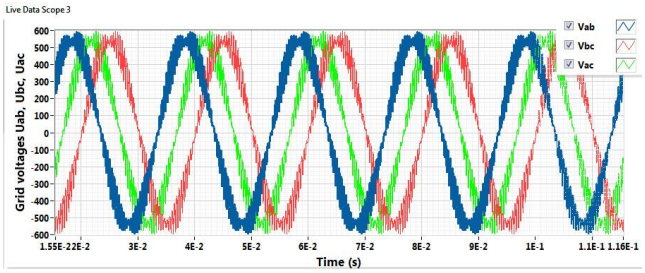

Fig. 14. Waveforms of line voltages U_{ab}, U_{bc}, U_{ac}

FPGA Desktop Execution Node has severe impact on the speed of simulation execution, and twofold impact on the simulation experience. On the one hand, 100 ms of simulation time can take up to an hour on decent desktop PC. On the other, this provides a possibility of online parameter change. Parameters of the load, for example, can be changed during simulation and results can be seen instantaneously. Simulation can be speeded up further more with step size parameters or maximum acceptable error trade off.

IV. Conclusion

This paper presents an Active Front End converter initial design procedure overview. Although current stage of development enables only islanding operation, in future work development of control algorithm part for grid-tie operation will be included. Its control algorithm is developed using LabVIEW and tested using LabVIEW add-ons.

Co-simulation showed up to be a valuable tool for the hardware and control system design, calculating parameters of the control algorithm and fine-tuning without a risk of damaging equipment. Time of development is reduced significantly and LabVIEW is suitable for this application, since algorithms that are executed on FPGA and desktop are written using the same graphical programming language.

ACKNOWLEDGEMENT

This work was supported by the Ministry of Science and Technological Development, Republic of Serbia (Project number: III 44006).

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